

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10550326
	Filing Date		2005-09-23
	First Named Inventor	Roger D. Chamberlain	
	Art Unit	2439	
	Examiner Name	Tolentino, Roderick	
	Attorney Docket Number	53047-57365	

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	6	5995963		1999-11-30	Nanba et al.	
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20	7224185	B2	2007-05-29	Campbell et al.	
21	7225188	B1	2007-05-29	Gai et al.	
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6	20040015633		2004-01-22	Smith	
7	20040054924		2004-03-18	Chuah et al.	
8	20040196905		2004-10-07	Yamane et al.	
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	17	20070078837		2007-04-05	Indeck et al.	
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10	2002082271	WO		2002-10-17	Audible Magic Corporation		<input type="checkbox"/>
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12	CLARK ET AL., "Scalable Pattern Matching for High Speed Networks", Proceedings of the 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2004; FCCM 2004, 20-23 April 2004; pp. 249-257; IEEE Computer Society; Cambridge, MA USA	<input type="checkbox"/>

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13	COMPTON ET AL., "Reconfigurable Computing: A Survey of Systems and Software", Technical Report, Northwestern University, Dept. of ECE, 1999, presented by Yi-Gang Tai	<input type="checkbox"/>
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15	DHARMAPURIKAR et al., "Deep Packet Inspection Using Parallel Bloom Filters," Symposium on High Performance Interconnects (HotI), Stanford, California, 2003, pp. 44-51	<input type="checkbox"/>
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35	ROY, "A bounded search algorithm for segmented channel routing for FPGA's and associated channel architecture issues", IEEE, Nov. 11, 1993, pp. 1695-1705, Vol. 12	<input type="checkbox"/>
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